Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (original): A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of series connected MOS transistors wherein at least one of said plurality of series connected MOS transistors is a NMOS transistor and at least one of said plurality of series connected MOS transistors is a PMOS transistor;

a precharge circuit connected to a clock signal, a circuit supply voltage, and said pull-down network;

a ground switch circuit connected to said clock signal and to said pull-down network; and

an output node which is connected to a common node of said pull-down network and said precharge circuit.

Claim 2 (original): The dynamic logic circuit of claim 1 wherein said precharge circuit comprises a PMOS transistor.

Claim 3 (original): The dynamic logic circuit of claim 1 wherein said ground switch circuit comprises a NMOS transistor.

Claim 4 (original): The dynamic logic circuit of claim 1 wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body.

Claim 5 (original): A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of series connected PMOS transistors;

a precharge circuit connected to a clock signal, a circuit supply voltage, and said pull-down network;

a ground switch circuit connected to said clock signal and to said pull-down network; and

an output node which is connected to a common node of said pull-down network and said precharge circuit.

Claim 6 (original): The dynamic logic circuit of claim 5 wherein said precharge circuit comprises a PMOS transistor.

Claim 7 (original): The dynamic logic circuit of claim 5 wherein said ground switch circuit comprises a NMOS transistor.

Claim 8 (currently amended): A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of series connected PMOS transistors ~~The dynamic logic circuit of claim 5~~ wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body~~.~~ ;

a precharge circuit connected to a clock signal, a circuit supply voltage, and said pull-down network;

a ground switch circuit connected to said clock signal and to said pull-down network; and

an output node which is connected to a common node of said pull-down network and said precharge circuit.

Claim 9 (original): A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel connected MOS transistors with a first and second common node, wherein at least one of said plurality of parallel connected MOS transistors is a NMOS transistor and at least one of said plurality of parallel connected MOS transistors is a PMOS transistor;

a precharge circuit connected to a clock signal and to said first common node of said pull-down network;

a ground switch circuit connected to said clock signal and to said second common node of said pull-down network; and

an output node which is connected to said first common node of said pull-down network.

Claim 10 (original): The dynamic logic circuit of claim 9 wherein said precharge circuit comprises a PMOS transistor.

Claim 11 (original): The dynamic logic circuit of claim 9 wherein said ground switch circuit comprises a NMOS transistor.

Claim 12 (Currently amended): A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel connected MOS transistors with a first and second common node, wherein at least one of said plurality of parallel connected MOS transistors is a NMOS transistor and at least one of said plurality of parallel connected MOS transistors is a PMOS transistor ~~The static logic circuit of claim 9 wherein~~ and at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body~~.~~ ;

a precharge circuit connected to a clock signal and to said first common node of said pull-down network;

a ground switch circuit connected to said clock signal and to said second common node of said pull-down network; and

an output node which is connected to said first common node of said pull-down network.

Claim 13 (original): A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel connected PMOS transistors with a first and second common node;

a precharge circuit connected to a clock signal and to said first common node of said pull-down network;

a ground switch circuit connected to said clock signal and to said second common node of said pull-down network; and

an output node connected to said first common node of said pull-down network.

Claim 14 (original): The dynamic logic circuit of claim 13 wherein said precharge circuit comprises a PMOS transistor.

Claim 15 (original): The dynamic logic circuit of claim 13 wherein said ground switch circuit comprises a NMOS transistor.

24

Claim 16 (Currently amended): A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel connected PMOS transistors with a first and second common node

~~The static logic circuit of claim 13~~ wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body~~.~~;

a precharge circuit connected to a clock signal and to said first common node of said pull-down network;

a ground switch circuit connected to said clock signal and to said second common node of said pull-down network; and

an output node connected to said first common node of said pull-down network.